ISSN 2394-3777 (Print)
ISSN 2394-3785 (Online)
Available online at www.ijartet.com

International Journal of Advanced Research Trends in Engineering and Technology (IJARTET)
Vol. II, Issue III, March 2015

High Speed and Reduced Area 16 bit Vedic Multiplier Using Carry Select Adder

D.Muthulakshmi[1], S.Durgadevi[2], B.Iyyappan[3]
PG scholar, E.G.S.Pillay engineering college, Nagapattinam[1]
Assistant Professor, E.G.S.Pillay Engineering College, Nagapattinam, [2]
VLSI Design Engineer Chennai[3]

Abstract---. Processors speed depends greatly on the speed of multipliers.This paper gives the novel method of multiplier using vedic mathematics that rediscovered from ancient maths.High speed 16 bit Vedic multiplier architecture which is quite different from the conventional method and vedic multiplier designed using carry select adder is proposed in this paper.Multiplier operation based on Urdhva Tiryakbhayam Sutra which is highly preferred algorithm for multiplication that increases multiplier speed by reduced iteration.

Keywords---Ripple Carry Adder (RCA), Vedic multiplier using RCA and Carry Select Adder (CSLA), Vedic mathematics, Urdhva Tiryakbhyam sutra**.**